IN THE CLAIMS:

Claims 1, 22, 43, and 64 have been amended herein. All of the pending Claims 1 through 84 are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

Listing of Claims:

1. (Currently Amended) A semiconductor die ~~having at least one circuit~~ connected to at least one component comprising:
the ~~a~~ semiconductor die having an active surface, an inactive surface, ~~and~~ at least one circuit[[:]], and at least one bond pad formed on a portion of the active surface and connected to the at least one circuit[[;]], the ~~and~~ at least one bond pad formed on a portion of the inactive surface of the semiconductor die for at least one of lowering stress of a portion of the semiconductor die, protecting a portion of the semiconductor die, ~~and~~ lowering stress of a portion of the semiconductor die, and protecting a portion of the semiconductor die by placing the at least one bond pad on a portion of the inactive surface of the semiconductor die distributing the forces therearound.

2. (Original) The semiconductor die of claim 1, wherein the at least one bond pad formed on the portion of the inactive surface of the semiconductor die includes a bond pad connected to the at least one circuit of the semiconductor die.

3. (Original) The semiconductor die of claim 1, wherein the at least one bond pad formed on the portion of the inactive surface includes a bond pad having more than one layer of material.

4. (Original) The semiconductor die of claim 3, wherein the at least one bond pad formed on the portion of the inactive surface includes a bond pad having more than one layer of material, each layer of material having a coefficient of thermal expansion different from a coefficient of thermal expansion of another layer of material.

5. (Original) The semiconductor die of claim 1, further comprising:

a substrate having a portion thereof connected to the at least one bond pad formed on the portion of the active surface of the semiconductor die, the substrate having at least one circuit connected to the at least one bond pad formed on the active surface of the semiconductor die; and

at least one bond wire connected to the at least one pad formed on the portion of the inactive surface of the semiconductor die.

6. (Original) The semiconductor die of claim 5, wherein the substrate includes a portion thereof located adjacent at least one edge of the semiconductor die.

7. (Original) The semiconductor die of claim 5, further comprising a sealant material located between a portion of the semiconductor die and a portion of the substrate.

8. (Original) The semiconductor die of claim 5, further comprising a sealant material located along a portion of at least one edge of the semiconductor die and a portion of the substrate.

9. (Original) The semiconductor die of claim 5, wherein the:

at least one bond pad formed on the portion of the active surface is connected to a contact pad on a portion of a surface of the substrate.

10. (Original) The semiconductor die of claim 5, further comprising:

at least one resilient connector attached to a portion of the active surface of the semiconductor die and a portion of a surface of the substrate.

11. (Original) The semiconductor die of claim 1, further comprising:
at least one resilient connector attached to a portion of the active surface of the semiconductor die and a portion of a surface of a substrate.

12. (Original) The semiconductor die of claim 1, wherein the at least one bond pad formed on the portion of the inactive surface of the semiconductor die includes a shape of one of a square shape, rectangular shape, circular shape, elliptical shape, hexagonal shape, and triangular shape.

13. (Original) The semiconductor die of claim 10, wherein the at least one resilient connector includes a shape of one of a square shape, rectangular shape, circular shape, elliptical shape, hexagonal shape, and triangular shape.

14. (Original) The semiconductor die of claim 5, wherein the substrate includes at least one resilient connector located on a surface thereon abutting a portion of the semiconductor die.

15. (Original) The semiconductor die of claim 1, wherein the semiconductor die includes at least a portion of one metal protection layer located on a portion of the active surface of the semiconductor die.

16. (Original) The semiconductor die of claim 1, wherein the semiconductor die includes a first passivation layer located on a portion thereof and a second passivation layer located on a portion of the first passivation layer.

17. (Original) The semiconductor die of claim 1, wherein the semiconductor die includes at least a portion of one metal protection layer located on a portion of the active surface of the semiconductor die, a first passivation layer located on a portion of the one metal protection layer, and a second passivation layer located on a portion of the first passivation layer.

18. (Original) The semiconductor die of claim 1, wherein the semiconductor die includes at least a portion of more than one metal protection layer located on a portion of the active surface of the semiconductor die, a first passivation layer located on a portion on the metal protection layer, and a plurality of passivation layers located on at least a portion of the first passivation layer.

19. (Original) The semiconductor die of claim 1, wherein the semiconductor die includes a portion of at least one metal protection layer having a portion thereof located adjacent an edge of the semiconductor die.

20. (Original) The semiconductor die of claim 1, wherein the semiconductor die includes at least one trace extending from at least a portion of the at least one bond pad formed on the portion of the active surface of the semiconductor die.

21. (Original) The semiconductor die of claim 20, further comprising at least one connector located on a portion of the at least one trace.

22. (Currently Amended) A semiconductor die having ~~at least one circuit~~ connected to at least one component and a substrate comprising:

the ~~a~~ semiconductor die having an active surface, an inactive surface and at least one circuit, the semiconductor die including at least one bond pad formed on a portion of the active surface thereof connected to the at least one circuit and at least one bond pad formed on a portion of the inactive surface for at least one of lowering stress of a portion of the semiconductor die, protecting a portion of the semiconductor die, and lowering stress of a portion of the semiconductor die by placing the at least one bond pad on a portion of the inactive surface of the semiconductor die distributing the forces therearound, and protecting a portion of the semiconductor die; and

a substrate having a portion thereof connected to the at least one bond pad formed on the portion of the active surface of the semiconductor die.

23. (Original) The semiconductor die and substrate of claim 22, wherein the at least one bond pad formed on the portion of the inactive surface of the semiconductor die includes a bond pad connected to the at least one circuit of the semiconductor die.

24. (Original) The semiconductor die and substrate of claim 22, wherein the at least one bond pad formed on the portion of the inactive surface includes a bond pad having more than one layer of material.

25. (Original) The semiconductor die and substrate of claim 24, wherein the at least one bond pad formed on the portion of the inactive surface includes a bond pad having more than one layer of material, each layer of material having a coefficient of thermal expansion different from a coefficient of thermal expansion of another layer of material.

26. (Original) The semiconductor die and substrate of claim 22, further comprising: at least one bond wire connected to the at least one bond pad formed on the portion of the inactive surface of the semiconductor die.

27. (Original) The semiconductor die and substrate of claim 26, wherein the substrate includes a portion thereof located adjacent at least one edge of the semiconductor die.

28. (Original) The semiconductor die and substrate of claim 26, further comprising a sealant material located between a portion of the semiconductor die and a portion of the substrate.

29. (Original) The semiconductor die and substrate of claim 26, further comprising a sealant material located along a portion of at least one edge of the semiconductor die and a portion of the substrate.

30. (Original) The semiconductor die and substrate of claim 26, wherein the: at least one bond pad formed on the portion of the active surface is connected to a contact pad on a portion of a surface of the substrate.

31. (Original) The semiconductor die and substrate of claim 26, further comprising: at least one resilient connector attached to a portion of the active surface of the semiconductor die and a portion of a surface of the substrate.

32. (Original) The semiconductor die and substrate of claim 22, further comprising: at least one resilient connector attached to a portion of the active surface of the semiconductor die and a portion of a surface of the substrate.

33. (Original) The semiconductor die and substrate of claim 22, wherein the at least one bond pad formed on the portion of the inactive surface of the semiconductor die includes a shape of one of a square shape, rectangular shape, circular shape, elliptical shape, hexagonal shape, and triangular shape.

34. (Original) The semiconductor die and substrate of claim 32, wherein the at least one resilient connector includes a shape of one of a square shape, rectangular shape, circular shape, elliptical shape, hexagonal shape, and triangular shape.

35. (Original) The semiconductor die and substrate of claim 26, wherein the substrate includes at least one resilient connector located on a surface thereof abutting a portion of the semiconductor die.

36. (Original) The semiconductor die and substrate of claim 22, wherein the semiconductor die includes at least a portion of one metal protection layer located on a portion of the active surface of the semiconductor die.

37. (Original) The semiconductor die and substrate of claim 22, wherein the semiconductor die includes a first passivation layer located on a portion thereof and a second passivation layer located on a portion of the first passivation layer.

38. (Original) The semiconductor die and substrate of claim 22, wherein the semiconductor die includes at least a portion of one metal protection layer located on a portion of the active surface of the semiconductor die, a first passivation layer located on a portion of the one metal protection layer, and a second passivation layer located on a portion of the first passivation layer.

39. (Original) The semiconductor die and substrate of claim 22, wherein the semiconductor die includes at least a portion of more than one metal protection layer located on a portion of the active surface of the semiconductor die, a first passivation layer located on a portion of the more than one metal protection layer, and a plurality of passivation layers located on at least a portion of the first passivation layer.

40. (Original) The semiconductor die and substrate of claim 22, wherein the semiconductor die includes a portion of at least one metal protection layer having a portion thereof located adjacent an edge of the semiconductor die.

41. (Original) The semiconductor die and substrate of claim 22, wherein the semiconductor die includes at least one trace extending from at least a portion of the at least one bond pad formed on the portion of the active surface of the semiconductor die.

42. (Original) The semiconductor die and substrate of claim 41, further comprising at least one connector located on a portion of the at least one trace.

43. (Currently Amended) A method of relieving forces on a semiconductor die comprising:

forming an area of metal on a surface of the semiconductor die for one of decreasing stress acting on the surface of the semiconductor die by placing at least one bond pad on an inactive surface of the semiconductor die distributing the forces therearound and protecting at least a portion of the semiconductor die.

44. (Original) The method of claim 43, further comprising;

providing a substrate;

connecting the area of metal to a portion of the substrate; and

applying a force between the substrate and the area of metal.

45. (Original) The method of claim 43, further comprising:

applying a layer of material to passivate a portion of the area of metal.

46. (Original) The method of claim 43, wherein the area of metal comprises at least one bond pad formed on a portion of an inactive surface of the semiconductor die connected to a circuit of the semiconductor die.

47. (Original) The method of claim 46, wherein the at least one bond pad formed on a portion of the inactive surface includes a bond pad having more than one layer of material.

48. (Original) The method of claim 47, wherein the at least one bond pad formed on a portion of the inactive surface includes a bond pad formed having more than one layer of material, each layer of material having a different coefficient of thermal expansion than another layer of material.

49. (Original) The method of claim 46, further comprising:

forming a substrate having a portion thereof connected to the at least one bond pad formed on a portion of the inactive surface of the semiconductor die, the substrate having at least one circuit connected to the at least one bond pad of the semiconductor die; and

at least one bond wire connected to the at least one bond pad formed on the inactive surface of the semiconductor die.

50. (Original) The method of claim 49, wherein the substrate includes a portion thereof located adjacent at least one edge of the semiconductor die.

51. (Original) The method of claim 49, further comprising applying a sealant material located between a portion of the semiconductor die and a portion of the substrate.

52. (Original) The method of claim 49, further comprising applying a sealant material located along a portion of at least one edge of the semiconductor die and a portion of the substrate.

53. (Original) The method of claim 49, further comprising:

connecting the at least one bond pad formed on the inactive surface to a contact pad on a portion of a surface of the substrate.

54. (Original) The method of claim 49, further comprising:

attaching at least one resilient connector to a portion of the active surface of the semiconductor die and a portion of a surface of the substrate.

55. (Original) The method of claim 49, wherein the at least one bond pad formed on the inactive surface of the semiconductor die includes a shape of one of a square shape, rectangular shape, circular shape, elliptical shape, hexagonal shape, and triangular shape.

56. (Original) The method of claim 49, wherein the substrate includes at least one resilient connector located on a surface thereon abutting a portion of the semiconductor die.

57. (Original) The method of claim 43, wherein the semiconductor die includes at least a portion of one metal protection layer located on a portion of an active surface thereof.

58. (Original) The method of claim 43, wherein the semiconductor die includes a first passivation layer located on a portion thereof and a second passivation layer located on a portion of the first passivation layer.

59. (Original) The method of claim 43, wherein the semiconductor die includes at least a portion of one metal protection layer located on a portion of an active surface thereof, a first passivation layer located on a portion of the one metal protection layer, and a second passivation layer located on a portion of the first passivation layer.

60. (Original) The method of claim 43, wherein the semiconductor die includes at least a portion of more than one metal protection layer located on a portion of an active surface thereof, a first passivation layer located on a portion of the more than one metal protection layer, and a plurality of passivation layers located on at least a portion of the first passivation layer.

61. (Original) The method of claim 43, wherein the semiconductor die includes a portion of at least one metal protection layer located adjacent an edge of the semiconductor die.

62. (Original) The method of claim 43, wherein the semiconductor die includes at least one trace extending from at least a portion of the area of metal formed on the surface of the semiconductor die.

63. (Original) The method of claim 62, further comprising at least one connector located on a portion of the at least one trace.

64. (Currently Amended) A method of forming a semiconductor die ~~having at least one circuit~~ connected to at least one component and a substrate comprising:

providing a semiconductor die having an active surface and an inactive surface, the semiconductor die including at least one bond pad formed on a portion of the active surface connected to the at least one circuit and at least one bond pad formed on a portion of the inactive surface;

performing ~~for~~ at least one of lowering stress of a portion of the semiconductor die, protecting a portion of the semiconductor die, ~~and~~ lowering stress of a portion of the semiconductor die by placing the at least one bond pad on a portion of the inactive surface of the semiconductor die distributing the forces therearound, and protecting a portion of the semiconductor die; and

attaching a substrate having a portion thereof connected to the at least one bond pad formed on the portion of the active surface of the semiconductor die.

65. (Original) The method of claim 64, wherein the at least one bond pad formed on the portion of the inactive surface of the semiconductor die includes a bond pad connected to a circuit of the semiconductor die.

66. (Original) The method of claim 64, wherein the at least one bond pad formed on the portion of the inactive surface includes a bond pad having more than one layer of material.

67. (Original) The method of claim 66, wherein the at least one bond pad formed on the portion of the inactive surface includes a bond pad having more than one layer of material, each layer of material having a different coefficient of thermal expansion than another layer of material.

68. (Original) The method of claim 64, further comprising:

connecting at least one bond wire to the at least one bond pad formed on the inactive surface of the semiconductor die.

69. (Original) The method of claim 68, wherein the substrate includes a portion thereof located adjacent at least one edge of the semiconductor die.

70. (Original) The method of claim 66, further comprising applying a sealant material located between a portion of the semiconductor die and a portion of the substrate.

71. (Original) The method of claim 66, further comprising applying a sealant material located along a portion of at least one edge of the semiconductor die and a portion of the substrate.

72. (Original) The method of claim 66, further comprising:
connecting the at least one bond pad formed on the portion of the active surface of the semiconductor die to a contact pad on a portion of a surface of the substrate.

73. (Original) The method of claim 66, further comprising:
attaching at least one resilient connector to a portion of the active surface of the semiconductor die and a portion of a surface of the substrate.

74. (Original) The method of claim 64, further comprising:
attaching at least one resilient connector to a portion of the active surface of the semiconductor die and a portion of a surface of the substrate.

75. (Original) The method of claim 64, wherein the at least one bond pad formed on the inactive surface of the semiconductor die includes a shape of one of a square shape, rectangular shape, circular shape, elliptical shape, hexagonal shape, and triangular shape.

76. (Original) The method of claim 74, wherein the at least one resilient connector includes a shape of one of a square shape, rectangular shape, circular shape, elliptical shape, hexagonal shape, and triangular shape.

77. (Original) The method of claim 68, wherein the substrate includes at least one resilient connector located on a surface thereon abutting a portion of the semiconductor die.

78. (Original) The method of claim 64, wherein the semiconductor die includes at least a portion of one metal protection layer located on a portion of the active surface thereof.

79. (Original) The method of claim 64, wherein the semiconductor die includes a first passivation layer located on a portion thereof and a second passivation layer located on a portion of the first passivation layer.

80. (Original) The method of claim 64, wherein the semiconductor die includes at least a portion of one metal protection layer located on a portion of the active surface thereof, a first passivation layer located on a portion of the one metal protection layer, and a second passivation layer located on a portion of the first passivation layer.

81. (Original) The method of claim 64, wherein the semiconductor die includes at least a portion of more than one metal protection layer located on a portion of the active surface thereof, a first passivation layer located on a portion of the more than one metal protection layer, and a plurality of passivation layers located on at least a portion of the first passivation layer.

82. (Original) The method of claim 64, wherein the semiconductor die includes a portion of at least one metal protection layer located adjacent an edge thereof.

83. (Original) The method of claim 64, wherein the semiconductor die includes at least one trace extending from at least a portion of the at least one bond pad formed on the active surface of the semiconductor die.

84. (Original) The method of claim 83, further comprising at least one connector located on a portion of the at least one trace.